REMARKS

First, Applicant notes that Tanaka is superficially similar to Applicant's claimed invention, and Tanaka's details, including its mathematical signal descriptions, must be considered to appreciate that Applicant's invention as claimed differs from Tanaka in fundamental and patentably distinct ways. Applicant has made a good faith effort to set forth at least some of these differences using simple, accurate language. If for any reason the examiner disagrees with any of the differences argued below, Applicant respectfully requests that the Patent Office provide technically detailed arguments that are consistent with the teachings of Tanaka.

With the above in mind, Applicant respectfully requests that the Patent Office withdraw all anticipation rejections based on Tanaka (US 5,909,148) because, among other errors, the basis for alleging anticipation depends on the mistaken identification of the signal generated by Tanaka's Numeric Controlled Oscillator (NCO) 9 as meeting Applicant's claim limitations involving PLL output signal generation. Tanaka's illustrations and its description of NCO 9 at col. 5, lines 43-52 irrefutably contradicts the Office's assertion that the signal generated by NCO 9 can "inherently" be taken as an "output signal" within the meaning of Applicant's claims. The signal generated by NCO 9 may be an output signal with respect to NCO 9, but it is not an output signal of the AFC / PLL circuit in which NCO 9 resides, nor would one skilled in the art ever understand the NCO 9 signal as an output signal. Indeed, Tanaka plainly illustrates the DEMODULATED SIGNAL output by phase detector 10 as its AFC / PLL output signal, and the Office does not account for this contradiction to its arguments.

Arguing over whether the NCO 9 signal is an output signal within the meaning of Applicant's claims is not a simple matter of the Office giving claim terms their broadest reasonable interpretation; rather it represents an argument over whether the Office

legally can use the term "output signal" in a context that is at odds with the meaning of that term as used in Applicant's claims and with the meaning that one of ordinary skill in the art would assign to that term. As a matter of law the Office is obligated to construe the claim terms consistent with the meanings that one skilled in the art would assign. In re Cortright, 165 F.3d 1353, 49 U.S.P.Q.2d 1464 (Fed. Cir. 1999). The Office is further obligated to construe claim terms consistent with the specification. In re Hyatt, 211 F.3d 1367, 54 U.S.P.Q.2d 1664 (Fed. Cir. 2000).

In all claims at issue—including all independent claims 1, 10, and 24—one skilled in the art would unambiguously understand that Applicant's claimed output signal refers to an overall or final PLL output signal. (Applicant amended independent claims 1 and 24 as a precaution, to ensure that the claimed output signal is unambiguously understood to be an overall PLL output signal. Independent claim 10 as originally filed is unambiguous on that point.) Further, the instant application's Summary and its detailed description of Figs. 3, 4, and 5 make clear that the claimed output signal is the overall output signal of interest from Applicant's PLL circuit, to be used by downstream circuitry.

Therefore, it is legal error for the Office to argue that the NCO 9 signal inherently is an output signal within the meaning of Applicant's claims. The signal generated by NCO 9 may be an "output" with respect to NCO 9, but it plainly is not an output with respect to the AFC / PLL circuit in which NCO 9 resides, and it plainly is not an output signal within the meaning of Applicant's claims. As such, the Office should withdraw its rejections of claims 1-7, 10, 11, 13-16, 18, 24-26, 32, and 37 as being anticipated under 35 U.S.C. § 102(b) by Tanaka.

As a further failing of the Tanaka-based anticipation rejections, all claims at issue include specific limitations regarding the generation of the PLL output signal as a function of averaged control values determined from the phase differences between the

PLL output signal and a PLL input reference signal. (Claim 1 is amended herein to clarify the bearing averaged control values have on PLL output signal generation, and claims 10 and 24 are unambiguous as filed.) For example, claim 1 requires "adapting a filter used to filter said successive phase difference values based on average control values determined from said successive control values," wherein the control values are themselves determined from the successive phase differences of the PLL input and output signals. Independent claims 10 and 24 include similarly explicit limitations.

Item 3 of the Office Action erroneously argues that Tanaka meets the phase difference and average control value limitations of Applicant's claims, by mistakenly arguing that: (a) element 9 in Fig. 1 generates Applicant's claimed PLL output signal; (b) element 6 in Fig. 2—there is no element 6 in Fig. 2—provides Applicant's claimed PLL input (reference) signal; (c) element 8 in Fig. 1 generates successive phase differences between the PLL input and output signals in the manner claimed by Applicant; (d) element 11 in Fig. 1 generates Applicant's claimed control values; and (e) that elements 13, 14, 15, 16, 101 and 102 of Fig. 1 teach adapting control value filtering based on average control values.

First, as argued extensively above, element 9 does not produce the claimed PLL output signal, therefore element 8, which is disclosed only as receiving signals from elements 6 and 9 cannot by definition produce the claimed successive phase differences between PLL input and output signals.

Second, as explicitly explained by Tanaka at col. 5, line 13-26, the output of the (loop) filter 11 is proportional to the oscillation frequency of NCO 9, rather than being a function of successive control values within the meaning of Applicant's claims. Further, Tanaka discloses that filter 11 is updated not as a function of average control values, but rather as a function of a time change amount $\Delta g(nT)$, which is determined by a delaying

device 13, a subtracting circuit 14, and an averaging circuit 15. While the Office argues that this is the same as Applicant's claimed averaging-based control, that argument glosses over differences which cannot be overlooked in an anticipation analysis. That is, Tanaka explicitly teaches the output of filter 11 as being proportional to the oscillator frequency of NCO 9, not proportional to successive phase differences between input and output signals. Further Tanaka explains that filter 11 is updated by subtracting a delayed version of the filter 11 output signal from a current version. It is these "delta" signal values which are averaged by averaging circuit 15 to produce the filter adaptation of Tanaka.

With the above points in mind, and recognizing that additional distinctions can be made between the operational details of Applicant's claimed invention and Tanaka, Applicant respectfully submits that all claims patentably define over Tanaka and, therefore, that all anticipation rejections based on Tanaka should be withdrawn. Because the pending independent claims define over Tanaka, Applicant submits that all anticipation rejections of dependent claims fail as a matter of law, as do all obviousness rejections of various ones of the dependent claims. (All obviousness rejections depend on the same alleged teachings of Tanaka as used in making out the anticipation rejections.)

In closing, Applicant notes with appreciation the Office's indication of allowable subject matter, and Examiner Wang's obvious desire to advance prosecution of this case on its merits after the misunderstanding regarding withdrawal of the prior Final Office Action. Applicant also wishes to advance this matter on its merits and welcomes the Office's next communication.

Respectfully submitted,

COATS & BENNETT, P.L.L.C.

Dated: February 27, 2006

Michael D. Murphy
Registration No.: 44,958

P.O. Box 5
Raleigh, NC 27602
Telephone: (919) 854-1844
Facsimile: (919) 854-2084